REMARKS

Claims 1-31 are pending. Claims 1-31 are rejected. Claims 1-11 were rejected under 35 USC 103(a) as being unpatentable over Self (5,623,644) in view of Booth (6,065,073) and further in view of Ren (Using Clustering for Effective Management of a Semantic Cache in Mobile Compuating). Claims 12-31 were rejected under 35 USC 103(a) as being unpatentable over Self in view of Kelly (5,379,440), Booth, Dervin (6,952,766), and Sgroi "Addressing the System-on-a-chip Interconnection Woes Through Communication-Based Design." The rejections are respectfully traversed, for the reasons cited below.

The independent claims have been amended to facilitate prosecution. The independent claims have been amended to recite "a first cluster including a first plurality of configuration space registers (CSRs), a first plurality of processors, a first plurality of memory banks, a first service processor, and a first interconnection controller, wherein each of the plurality of processors has a first point-to-point link to a corresponding memory bank, a second point-to-point link to the first service processor, and a third point-to-point link to the first interconnection controller." This amendment is supported in Figure 2 and associated description.

The Examiner in rejecting all independent claims relies on Self to describe point-to-point connections. However, neither Self nor any of the other cited references teaches or suggests "wherein each of the plurality of processors has a first point-to-point link to a corresponding memory bank, a second point-to-point link to the first service processor, and a third point-to-point link to the first interconnection controller." Self only shows a processor having a single point-to-point link to a memory controller. The memory controller is connected to a single memory bank. There are no "plurality of memory banks" or "service processor." By contrast, Figure 2 and associated description show "a first cluster including a first plurality of configuration space registers (CSRs), a first plurality of processors, a first plurality of memory banks, a first service processor, and a first interconnection controller, wherein each of the plurality of processors has a first point-to-point link to a corresponding memory bank, a second point-to-point link to the first service processor, and a third point-to-point link to the first interconnection controller." The recited architecture is believed to be novel and nonobvious over the cited art either alone or in combination.

Claim 1 has also been amended to recite "the second interconnection controller connected to the first interconnection controller, wherein indicators in the first plurality of CSRs are toggled to disconnect the second interconnection controller from the first interconnection controller." This recitation is supported in on page 19, lines 11-27. None of the cited references are believed to teach or suggest toggling any indicators in the first plurality of CSRs.

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants' Representative believes that all pending claims are allowable in their present form. If the Examiner has any questions or concerns for Applicants' Representative, the Examiner is encouraged to contact the Undersigned at the number provided below.

Respectfully submitted,
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